CLAIMS

1. A method of fabricating a CMOS inverter comprising: ^ 1 providing a heterostructure including a Si substrate, a relaxed Si_{1-x}Ge_x layer on said Si 2 substrate, and a strained surface layer on said relaxed Si_{1-x}Ge_x layer; and 3 integrating a pMOSFET and an nMOSFET in said heterostructure, wherein the channel 4 5 of said pMOSFET and the channel of said nMOSFET are formed in said strained surface layer. 6 2. The method of claim 1, wherein the heterostructure further comprises a planarized 1 2 surface positioned between the strained surface layer and the Si substrate. 3. The method of claim 1, wherein the surface roughness of the strained surface layer 1 is less than 1nm. 2 1 4. The method of claim 1, wherein the heterostructure further comprises an oxide layer positioned between the relaxed Si_{1-x}Ge_x layer and the Si substrate. 2 5. The method of claim 1, wherein the heterostructure further comprises a SiGe graded 1 buffer layer positioned between the relaxed Si_{1-x}Ge_x layer and the Si substrate. 2 6. The method of claim 1, wherein the strained surface layer comprises Si. 1 7. The method of claim 1, wherein 0.1 < x < 0.5. 1 8. The method of claim 7, wherein the ratio of gate width of the pMOSFET to the gate 1

- 2 width of the nMOSFET is approximately equal to the ratio of the electron mobility and the
- 3 hole mobility in bulk silicon.
- 9. The method of claim 7, wherein the ratio of gate width of the pMOSFET to the gate
- 2 width of the nMOSFET is approximately equal to the ratio of the electron mobility and the
- 3 hole mobility in the strained surface layer.
- 1 10. The method of claim 7, wherein the ratio of gate width of the pMOSFET to the
- 2 gate width of the nMOSFET is approximately equal to the square root of the ratio of the
- 3 electron mobility and the hole mobility in bulk silicon.
- 1 11. The method of claim 7, wherein the ratio of gate width of the pMOSFET to the
- 2 gate width of the nMOSFET is approximately equal to the square root of the ratio of the
- 3 electron mobility and the hole mobility in the strained surface layer.
- 1 12. The method of claim 7, wherein the gate drive is reduced to lower power
- 2 consumption.
- 1 13. A method of fabricating an integrated circuit comprising:
- 2 providing a heterostructure having a Si substrate, a relaxed Si_{1-x}Ge_x layer on said Si
- substrate, and a strained layer on said relaxed Si_{1-x}Ge_x layer; and
- forming a p transistor and an n transistor in said heterostructure, wherein said strained
- 5 layer comprises the channel of said n transistor and said p transistor, and said n transistor and
- said p transistor are interconnected in a CMOS circuit.

- 1 14. The method of claim 13, wherein the heterostructure further comprises a
- 2 planarized surface positioned between the strained layer and the Si substrate.
- 1 15. The method of claim 13, wherein the surface roughness of the strained layer is less
- than 1nm.
- 1 16. The method of claim 13, wherein the heterostructure further comprises an oxide
- 2 layer positioned between the relaxed Si_{1.x}Ge_x layer and the Si substrate.
- 1 17. The method of claim 13, wherein the heterostructure further comprises a SiGe
- 2 graded buffer layer positioned between the relaxed Si_{1-x}Ge_x layer and the Si substrate.
- 1 18. The method of claim 13, wherein the strained layer comprises Si.
- 1 19. The method of claim 13, wherein 0.1 < x < 0.5.
- 1 20. The method of claim 13, wherein the CMOS circuit comprises a logic gate.
- 1 21. The method of claim 13, wherein the CMOS circuit comprises a NOR gate.
- 1 22. The method of claim 13, wherein the CMOS circuit comprises an XOR gate.
- 1 23. The method of claim 13, wherein the CMOS circuit comprises a NAND gate.
- 1 24. The method of claim 13, wherein the p-channel transistor serves as a pull-up
- 2 transistor in said CMOS circuit and the n-channel transistor serves as a pull-down transistor in
- 3 said CMOS circuit.

- 1 25. The method of claim 13, wherein the CMOS circuit comprises an inverter.
- 26. A method of fabricating a CMOS inverter comprising:
- 2 providing a graded Si_{1-x}Ge_x layer on a first Si substrate;
- providing a relaxed Si_{1-v}Ge_v layer on said graded layer to form a first structure;
- bonding said relaxed layer of said first structure to a second structure that includes a
- 5 second Si substrate;
- 6 removing said first Si substrate and said graded layer;
- 7 providing a strained surface layer on said relaxed layer to form a heterostructure; and
- 8 integrating a pMOSFET and an nMOSFET in said heterostructure, wherein the
- 9 channel of said pMOSFET and the channel of said nMOSFET are formed in said strained
- 10 surface layer.
 - 1 27. A method of fabricating an integrated circuit comprising:
 - 2 providing a graded Si_{1-x}Ge_x layer on a first Si substrate;
 - providing a relaxed Si_{1-v}Ge_v layer on said graded layer to form a first structure;
 - 4 bonding said relaxed layer of said first structure to a second structure that includes a
 - 5 second Si substrate;
 - removing said first Si substrate and said graded layer;
 - 7 providing a strained surface layer on said relaxed layer to form a heterostructure; and
 - 8 forming a p transistor and an n transistor in said heterostructure, wherein said strained
 - 9 layer comprises the channel of said n transistor and said p transistor, and said n transistor and

said p transistor are interconnected in a CMOS circuit.